REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1 and 4-18 are pending in this case. Claims 1 and 4 are amended, and Claims 5-18 are added by the present amendment. Claims 1 and 4-18 are supported by the original disclosure and add no new subject matter.[1]

The outstanding Office Action rejected Claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent Publication No. 05-109977 (herein "JP977") in view of Yoshida et. al. (US Patent No. 5,821,625, herein "Yoshida") and Mimura et. al. (US Patent No. 5,805,865, herein "Mimura"). Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP977 in view of Yoshida and Mimura and in further view of Japanese Patent Publication No. 08-167703 (herein "JP703").

Applicant and Applicant's representatives thank Examiner Crane for the courtesy of an interview with Applicant's representatives on February 15, 2007. During the interview, Examiner Crane seemed to indicate that the cited references do not teach or suggest transmitting data from one chip through another to an external electrode. Applicant respectfully submits that the amended independent claims describe transmitting data from a memory chip through a CPU chip to an external electrode. In addition, the newly added dependent claims clarify the transfer of data from one semiconductor chip to the other. As such and in light of the following discussion, Applicant respectfully submits that favorable reconsideration of the application is warranted.

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP977 in view of Yoshida and Mimura. As Claim 2 is cancelled, the rejection of that claim is believed to be moot. Applicant respectfully traverses the rejection of Claim 1.

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[1] *See* Specification at page 1, line 20, to page 2, line 2, page 11, lines 1-14, and page 13, line 20, to page 14, line 6.

Amended Claim 1 recites a semiconductor device comprising a CPU block and a memory element block stacked including

> a first electrode portion for connecting to an external electrode through wiring,

and

> a third electrode portion having micro bumps **for providing a data connection** from said memory block in said first semiconductor chip to said CPU block in said second semiconductor chip,

wherein,

> the second electrode portion in said first semiconductor chip and the fourth electrode portion in said second semiconductor chip are arranged in a vicinity of a peripheral portion on each chip and the third electrode portion in said first semiconductor chip and the fifth electrode portion in said second semiconductor chip are arranged in a vicinity of a center portion on each chip.

JP977 describes connecting IC chip A and IC chip B, where IC chip A has a smaller pad size than IC chip B, in a manner that eliminates the vacant space of IC chip B and provides more input/output ports for IC chip A. In addition, the outstanding Office Action contained interpretations of several portions of JP977. The outstanding Office Action cited element 2 of JP977 as "a second electrode portion" and referred to the center of the bottom chip, IC chip B. The outstanding Office Action cited element 2 shown in a square in figure 3(a) of JP977 as "a third electrode pattern". The Office Action cited element 5 in the center of the top chip, IC chip A, as "a fourth electrode portion", and element 5 shown in a square in figure 3(c) of JP977 as "a fifth electrode portion". The outstanding Office Action asserted that the fourth electrode portion connects to the second electrode portion and the fifth electrode portion connects to the third electrode portion. However, JP977 does not teach or suggest several elements recited in Claim 1.

First, JP977 does not teach or suggest an electrode for providing a **"data connection** from said memory block in said first semiconductor chip to said CPU block in said second semiconductor chip." JP977 does not appear to teach or suggest that element 2 of JP977 provides any data connection between a block of memory elements in a first semiconductor chip and a CPU block in a second semiconductor chip.

Second, the square shape labeled as 2 in figure 3(a) of JP977 and referred to as "a third electrode pattern" in the outstanding Office Action is not at the periphery of IC chip B. Therefore, JP977 does not teach or suggest "the second electrode in said first semiconductor chip and the fourth electrode in said second semiconductor chip are arranged in a vicinity of a peripheral portion on each chip." Instead, the electrodes at the periphery of IC chip B, labeled as 1 on figure 3(a) of JP977, are connected by wiring 4 to the center of IC chip B, referred to as "a second electron portion" in the outstanding Office Action, and, thus, to the center of IC chip A, referred to as "a fourth electrode portion" in the outstanding Office Action. Consequently, JP977 describes a connection between ***an electrode at the peripheral portion of IC chip B and an electrode in the center of IC chip A***.

Third, JP977 does not teach or suggest a semiconductor device comprising ***a CPU block*** in a second semiconductor chip ***and a memory element block*** in a first semiconductor chip.

Fourth, JP977 describes a connection between IC chip A and IC chip B in an arbitrary location within the flat surface of IC chip A. JP977 does not teach or suggest connecting a first semiconductor chip and a second semiconductor chip as described in Claim 1.

Finally, with regard to the assertion made in the outstanding Office Action with respect to Claim 2, it is respectfully cited that ***all*** claim elements must be taught or suggested by the cited references to create a *prima facie* case of obviousness.[2] As JP977 does ***not*** teach

[2] MPEP § 2142.

or suggest the above-discussed elements of Claim 1, Claim 1 is patentable over JP977. Further, it is respectfully submitted that Yoshida and Mimura do not cure the deficiencies of JP977. As such, Claim 1 is patentable over JP977 in view of Yoshida and Mimura.

Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP977 in view of Yoshida and Mimura and in further view of JP703. As Claim 3 is cancelled, the rejection of that claim is believed to be moot. Claim 4 depends from Claim 1. Therefore, Claim 4 is patentable for at least the reasons discussed above with respect to Claim 1. Further, JP703 does not cure the deficiencies of JP977, Yoshida and Mimura. JP703 describes a CPU on one chip connected to memory elements on another, but JP703 does not teach connecting the two chips in the manner recited by Claim 1. In addition, the assertion in the outstanding Office Action that "the number of pad and bump arrangements would have to be 'corresponding' somehow 'to the number of bits of a memory.'" is insufficient to establish a *prima facie* case for obviousness based on JP703. In fact, no portion of JP703 is cited to support this conclusion. Consequently, Claim 4 is patentable over JP977 in view of Yoshida and Mimura and in further view of JP703.

New Claims 5-10 are supported in the original disclosure.[3] Claims 5-10 depend from Claim 1. Therefore Claims 5-10 are patentable for at least the reasons discussed above with respect to Claim 1.

New Claims 11-18 are supported in the original disclosure.[4] Claim 11 recites a semiconductor device comprising a CPU block and a memory element block stacked, including:

> a third electrode having micro bumps configured to provide a data connection from said memory block in said first semiconductor chip to said CPU block in said second semiconductor chip

[3] See specification at page 5, line 19 to page 6, line 18 and page 13, line 20, to page 14, line 6.
[4] See specification at page 5, line 19 to page 6, line 18 and page 13, line 20, to page 14, line 6.

wherein,

> the second electrode in said first semiconductor chip and the fourth electrode in said second semiconductor chip are located in a vicinity of a peripheral portion on each chip, and
> the third electrode in said first semiconductor chip and the fifth electrode in said second semiconductor chip are located in a vicinity of a center portion on each chip.

As noted above, JP977 does not teach or suggest a data connection between a block of memory elements in a first semiconductor chip and a CPU block in a second semiconductor chip. JP977 does not teach or suggest exchanging data between a memory element block and a CPU block through micro bumps or connecting two semiconductor chips in the manner quoted above. Therefore, Claim 11 (and all claims dependent therefrom) are patentable over JP977. Because Yoshida and Mimura do not cure the deficiencies of JP977, Claim 11 (and all claims dependent therefrom) are patentable over JP977 in view of Yoshida and Mimura.

Accordingly, the outstanding rejections are traversed and the pending claims are believed to be in condition for formal allowance. An early and favorable action to that affect is, therefore, respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Edward Tracy

Bradley D. Lytle
Attorney of Record
Registration No. 40,073

Edward W. Tracy, Jr.
Registration No. 47,998

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)